Vivekananda Global University, Jaipur (Effective from session 2018-19)

M. Tech (VLSI Design) **Semester I**

MBM 204: RESEARCH METHODOLOGY

3L-0T-0P-3C **M.M.100**

Module – I: **Meaning and Importance of Research** – Types of Research- Exploratory Research – Descriptive Research – Casual Research - Research Approaches- Research Process ––Defining Research Problem- Selection and necessity of defining the problem.

Module – II: **Research Design** –meaning, need and features of good research design- Important concepts related to research design. Experimental research designs: Before and After without control design, After only with control design, Before and after with control design, Completely randomized design (C.R Design) .

Sampling and Sampling Design – Sampling Methods – Simple Random Sampling – Stratified Sampling – Systematic Sampling – Cluster Sampling – Multistage Sampling, Non–Probability Sampling – Convenience Sampling – Judgment Sampling – Quota Sampling- Snowball sampling.

Module – III: **Data Collection** – Primary and Secondary Data – Designing of Questionnaire –**Measurement and Scaling** – Nominal Scale – Ordinal Scale – Interval Scale – Ratio Scale –Guttman Scale – Likert Scale – Schematic Differential Scale. Descriptive statistics- Measures of central tendency- Dispersion- Skewness -Correlation and Regression Analysis.

Module – IV: **Editing** – Coding – Classification of Data – Tables and Graphic Presentation –Basics of inferential statistics- Types of Errors- **Hypothesis testing** -Parametric test - T-test, Z test, Chi Square test- ANOVA Test. Introduction of SPSS.

Module – V: **Non Parametric Tests** – Kolmogorov – Smirnov Test – Runs Test for Randomness. Sign Test – Median Test –Factor Analysis.

Preparation and Presentation of Research Report- Types of reports- Layout of Research Report- Bibliography-References writing- Precautions for writing Research Report.

Suggested Books:

1. Mark Saunders, Philip Lewis, Adrian Thornbill, Research Methods for Business Students, Pearson,ND
2. Churchill, Iacobucci & Israel, Marketing Research: A South Asian Perspective, Cengage, New Delhi
3. C.R. Kothari, Research Methodology, New Age International.
4. Carver & Nash, Data Analysis with SPSS, Cengage, New Delhi
5. Alan Bryman & Emma Bell, Business Research Methods, Oxford University Press.
6. Donald R. Cooper & Pamela S. Schindler, Business Research Methods 8th Edition, Tata McGraw Hill.
7. K.V.S. Sarma, Statistics made sample, do it yourself on PC, Prentice Hall.

Vivekananda Global University, Jaipur (Effective from session 2018-19)

M. Tech (VLSI Design) **Semester I**

MDC 101 ADVANCE DIGITAL SIGNAL PROCESSING

3L-1T-0P-3.5C **M.M.100**

Module 1: MULTIRATE DIGITAL SIGNAL PROCESSING - Review of DFT, FFT, IIR Filters, FIR Filters,Introduction, Decimation by a Factor D, Interpolation by a Factor I, Sampling Rate Conversion by a Rational Factor I/D, Filter Design and Implementation for sampling rate Conversion Multistage Implementation of Sampling Rate Conversion, Applications of Multirate Signal Processing, Sampling Rate Conversion of Band pass Signals

Module 2: LINEAR PREDICTION AND OPTIMUM LINEAR FILTERS - Innovations Representation of a Stationary Random Process, Forward and Backward linear prediction, Solution of the Normal Equations, Properties of linear prediction-Error Filter, AR Lattice and ARMA Lattice-Ladder Filters.

Module 3: POWER SPECTRAL ESTIMATION - Estimation of Spectra from Finite Duration Observations of a signal, the Periodogram, Use DFT in power Spectral Estimation, Bartlett, Welch and Blackman, Tukey methods, Comparison of performance of Non-Parametric Power Spectrum Estimation Methods

Module 4: SPEECH SIGNAL PROCESSING - Digital models for speech signal : Mechanism of speech production – model for vocal tract, radiation and excitation – complete model – time domain processing of speech signal:- Pitch period estimation – using autocorrelation function – Linear predictive Coding: Basic Principles – autocorrelation method – Durbin recursive solution.

Module 5: WAVELET TRANSFORMS - Fourier Transform: Its power and Limitations – Short Time Fourier Transform – The Gabor Transform - Discrete Time Fourier Transform and filter banks – Continuous Wavelet Transform – Wavelet Transform Ideal Case – Perfect Reconstruction Filter Banks and wavelets – Recursive multi-resolution decomposition – Haar Wavelet – Daubechies Wavelet.

Text/ Reference Books:

1. John G.Proakis, Dimitris G.Manobakis, Digital Signal Processing, Principles, Algorithms and Applications, Third edition, (2000) PHI.
2. Monson H.Hayes – Statistical Digital Signal Processing and Modeling, Wiley, 2002.
3. L.R.Rabiner and R.W.Schaber, Digital Processing of Speech Signals, Pearson Education (1979).
4. Roberto Crist, Modern Digital Signal Processing, Thomson Brooks/Cole (2004)
5. Raghuveer. M. Rao, Ajit S.Bopardikar, Wavelet Transforms, Introduction to Theory and applications, Pearson Education, Asia, 2000.
6. Digital Signal Processing, Sanjit K Mitra, TMH
7. Digital Signal Processing, S.Salivahanan A Vallavaraj, C.Gnanapriya, TMH
8. Digital Signal Processing, A.V. Oppenheim and R.W. Schaffer, PHI
9. Digital Signal Processing, Thomas J. Cavicchi, John Wiley & Sons
10. Digital Signal Processing, Emmanuel Ifeachor, Barry Jervis, Pearson

Vivekananda Global University, Jaipur (Effective from session 2018-19)

M. Tech (VLSI Design) **Semester I**

MVL 101 ALGORITHMS FOR VLSI DESIGN AUTOMATION

3L-1T-0P-3.5C **M.M.100**

Module 1: VLSI PHYSICAL DESIGN AUTOMATION AND FABRICATION - VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI Automation Algorithms Partitioning - Problem formulation, classification of Partitioning algorithms, Group migration algorithms, simulated annealing.

Module 2: FLOOR PLANNING & PIN ASSIGNMENT - Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement Algorithms, recent trends in placement.

Module 3: GLOBAL ROUTING AND DETAILED ROUTING - Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

Module 4: OVER THE CELL ROUTING & VIA MINIMIZATION - Two layers over the cell routers, constrained & unconstrained via minimization

Compaction: Problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Module 5: VLSI SIMULATION

Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis- High level Synthesis.

High Level Synthesis

Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

Text/ Reference Books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
3. Rolf Drechsheler: "Evolutionary Algorithm for VLSI", Second edition
4. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.

Vivekananda Global University, Jaipur (Effective from session 2018-19)

M. Tech (VLSI Design) **Semester I**

MVL 111: DIGITAL SYSTEM DESIGN

3L-0T-0P-3C **M.M.100**

Module 1 Review of Combinational & Sequential Logic Design **Introduction to Programmable Logic Devices:** Overview of PLDs, Simple PLD, Complex PLD, Architecture of CPLD & FPGA

Module 2 **Integrated Circuit Logic family:** Evolution of TTL, IIL (merged structure), CML logic, 10K and 100K series of ECL, Stacked ECL, EFL

Module 3 MSI Logic Circuits: Derived logic building blocks such Decoders/ drivers, Encoders, Multiplexers, De-multiplexers, Magnitude Comparators, applications

MESFET, MESFET Inverter, DCFL, supper buffer FET logic, BFL

Module 4 **Memory Devices:** General memory operations, Programmable logic devices, Semi-conductor memories, SRAM, DRAM, FAMOS, FLOTOX

Module 5 **Testing & Verification:** Testing combinational circuits: Different fault models, path sensitization algorithm**Testing sequential circuits:** Sequential test methods; Functional & Timing simulation, delay models, boundary scan, faults, fault simulation, ATPG, BIST, DFT, Verification

Text / Reference Books:

1. R. J. Tocci : "Digital System: Principles & Applications" – PHI
2. Leo Chartrand, "Advanced Digital Systems: Experiments and Concepts with CPLDs", Cengage Learning.
3. John F. Wakerly, "Digital Design: Principles and Practices", Prentice Hall.
4. Charles H. Roth, "Fundamentals of Logic Design", 5th Ed., Cengage Learning.
5. M. Abramovici, M. A. Breuer & Arthur D," Digital Systems Testing & Testable Design", John-Wiley & Sons.

M. Tech (VLSI Design) **Semester I**

MVL 112 VLSI SIGNAL PROCESSING

3L-0T-0P-3C **M.M.100**

Module 1: Representation of DSP algorithms. Iteration Bound: Loop Bound Iteration Bound, Algorithms, and Iteration Bound for MultiMate data flow graphs.

Module 2: PIPELINING AND PARALLEL PROCESSING - Introduction, pipelining of FIR filters, parallel processing. Timing Techniques retiming: introduction, properties, and system inequalities, retiming techniques Unfolding: Introduction, algorithm, properties, critical path, and sample period reduction Folding: Introduction, Transformation, register minimization

Module 3: DSP ARCHITECTURES SYSTOLIC ARCHITECTURE DESIGN - Introduction, Design Methodologies, FIR systolic array, matrix matrix multiplication.

Module 4: FAST CONVOLUTION - Cook Toom, Winograd, Iterated convolution. Parallel FIR filters: Fast FIR, parallel architecture for rank order filters.

Module 5: Pipelining of recursive filters Introduction, pipeline interleaving, parallel processing in IIR filters, Scaling and round off noise computation, Bit level arithmetic architecture, parallel multipliers, bit serial multipliers, Canonic Singed digit arithmetic, distributed arithmetic.

Text/ Reference Books:

1. Keshab V Parhi, VLSI Digital Signal Processing, Willey India.

2. Peter Pirsch, Architecture for Digital Signal Processing, Wiley.

3. Magdy A Bayoumi, VLSI design methodologies for DSP architecture

MDC 111: ANTENNA THEORY AND TECHNIQUES

3L-0T-0P-3C **M.M.100**

Module: I. Review of the theory of electromagnetic radiation. Introduction to various antenna types wire, loop and helical antennas, analysis using assumed current distribution.

Module: II. Aperture antennas: slot, wave guide, horn, and reflector antennas. Analysis using field equivalence principle and Fourier transform methods. Linear arrays. Traveling wave & broadband antennas. Antenna measurements.

Module: III. Printed antennas: Feeding methods, transmission line & cavity models, analysis and design of rectangular & circular microstrip antenna.

Module: IV. Arrays: pattern synthesis, planar arrays, phased arrays. Active antennas and arrays. Paraboloidal reflector antenna, different feed configurations, shaped beam antennas, lens antenna.

Module: V. Antennas applications: Antennas for biomedical applications. Smart antennas for mobile communications. Antenna for infrared detectors.

Text/ Reference Books:

1. Antennas, John Kraus, Ronald Marhefka, Tmh
2. Electromagnetic Waves And Radiating Systems, E.C. Jordan And K.G. Balmain,Phi
3. Antenna Theory: Analysis and Design, Constantine A. Balanis, John Wiley & Sons
4. Antenna Theory & Design, Robert S. Elliott, John Wiley & Sons
5. Antennas And Wave Propagation,G. S. N. Raju , Pearson
6. Antennas and Wave Propagation, A.R. Harish, M. Sachidananda,
7. Antenna Theory and Practice, Chatterjee, R., New Age International

M. Tech (VLSI Design) **Semester III**

MDC 112 MIXED SIGNAL SYSTEM DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: INTRODUCTION - PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing, Example of Analog Mixed Signal Circuit Design

Module 2: DIGITAL SUB CIRCUITS - CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders. Digital Circuits like ALU, Comparator, and Parity generator, Timer, PWM, SRAM and DRAM, CAM

Module 3: ANALOG SUB CIRCUITS - Ideal Operational Amplifier, Inverting and Non-inverting configuration Differential amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier

Module 4: DATA CONVERTERS: DAC - Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs
ADC : Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit, Quantization error, Concept of over sampling, Counting ADC, Tracking ADC,Successive approximation ADC, Flash ADC, Dual Slope ADC

Module 5: OVER SAMPLING DATA CONVERTERS - Over sampling fundamentals, Delta –Sigma Converter basics, $\Delta\ \Sigma$ Modulator

Text/ Reference Books:

1. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3rd edition, John Wiley & Sons.
2. Jacob Baker, "CMOS Mixed-Signal circuit design", A John Willy & Sons, inc., publications, 2003.
3. Professor Bernhard Boser -"Analysis and Design of VLSI Analog-Digital Interface
4. Integrated Circuits" "Addison Wisely publications" (1991).
5. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley
6. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition
7. Ken Martin, Digital Integrated Circuit Design, John Wiley
8. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)
9. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits – A Design
10. Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition).
Sung-Mo Kang, Yusuf Le

Vivekananda Global University, Jaipur (Effective from session 2018-19)

M. Tech (VLSI Design) **Semester I**

MVL 113 ASIC DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: Introduction to ASICs , Types of ASICs , full custom ASIC , semi custom ASIC , standard cell based ASIC , gate array based ASIC , programmable ASIC , PLD , FPGA , Logical effort.

Module 2: Programmable ASICS, Programmable ASIC Logic cells, Anti fuse- static RAM, EPROM and EEPROM technology, PREP benchmarks, Actel ACT, Xilinx LCA, Altera FLEX, Altera MAX , Architecture of FPGAs (Xilinx Spartan-3 / Altera Cyclone-3).

Module 3: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES - EPROM to Realize a Sequential Circuit, Programmable Logic Devices, Designing a Synchronous Sequential Circuit using a GAL, EPROM, Realization State machine using PLD, FPGA, Xilinx FPGA, Xilinx 2000, Xilinx 3000.).

Module 4: System Design Using Verilog HDL (overview), Verilog Description of combinational Circuits, arrays, Verilog operators.

Module 5: Compilation and simulation of Verilog codes, modeling using Verilog. Flip Flops, registers, counters, sequential machine, combinational logic circuits, Verilog codes, serial adders.

Text/ Reference Books:

1. M.J.S. Smith, "Application – specific integrated circuits" – Addison – Wesley Longman Inc. 1997.

2. John M Yarbrough "Digital Logic applications and Design", Thomson Learning, 2001

3. Samir Palnitkar, "Verilog HDL", Pearson Education, 1996.

4. Data sheet: Spartan-3 FPGA Family Advanced Configuration Architecture – Xilinx XAPP452 (v1.1) June 25, 2008

5. Cyclone III Device Hand book, Volume 1

6. Andrew Brown, - "VLSI circuits and systems in silicon", Mc Graw Hill, 1991.

M. Tech (VLSI Design) **Semester I**

MVL 114: RF CIRCUIT DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: INTRODUCTION - Importance of Radiofrequency Design, RF Behavior of Passive Components, Chip Components and Circuit Board Considerations, General Transmission Line Equation, Micro strip Transmission Lines

Single- and Multiport Networks: Interconnecting Networks, Network Properties and Applications, Scattering Parameters

Module 2: RF FILTER - Basic Resonator and Filter Configurations, Special Filter Realizations, Filter Implementation, Coupled Filter

Active RF Components and Modeling: Semiconductor Basics, RF Diodes, Bipolar-Junction Transistor, RF Field Effect Transistors, High Electron Mobility Transistors, Diode Models, Transistor Models

Module 3: MATCHING AND BIASING NETWORKS - Impedance Matching Using Discrete Components, Micro strip Line Matching Networks, Amplifier Classes of Operation and Biasing Networks

Module 4: RF TRANSISTOR AMPLIFIER - Characteristics of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles, Broadband, High Power, and Multistage Amplifiers.

Module 5: OSCILLATORS AND MIXERS - Basic Oscillator Model, High Frequency Oscillator Configuration, Basic Characteristics of Mixers.

Text/ Reference Books:

1. Reinhold Ludwig, Pavel Bretchko, "*RF Circuit Design*", 1st Indian Reprint, 2001, PearsonEducation Asia

2. B Razavi, "Design of Analog CMOS Integrated Circuits", Mc Graw Hill, 2000

M. Tech (VLSI Design) **Semester I**

MDC 113: DIGITAL IMAGE PROCESSING

3L-0T-0P-3C **M.M.100**

Module 1: INTRODUCTION AND DIGITAL IMAGE FUNDAMENTALS - The origins of Digital Image Processing, Examples of Fields that Use Digital Image Processing, Fundamentals Steps in Image Processing, Elements of Digital Image Processing Systems, Image Sampling and Quantization, Some basic relationships like Neighbors, Connectivity, Distance Measures between pixels, Linear and Non Linear Operations.

Module 2: IMAGE ENHANCEMENT IN THE SPATIAL DOMAIN - Some basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic and Logic operations, Basics of Spatial Filters, Smoothening and Sharpening Spatial Filters, Combining Spatial Enhancement Methods. Image Enhancement in the Frequency Domain. Introduction to Fourier Transform and the frequency Domain, Smoothing and Sharpening Frequency Domain Filters, Homomorphic Filtering. Image Restoration.

Module 3: A MODEL OF THE IMAGE DEGRADATION - Restoration Process, Noise Models, Restoration in the presence of Noise Only Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering, Linear Position- Invariant Degradations, Estimation of Degradation Function, Inverse filtering, Wiener filtering, Constrained Least Square Filtering, Geometric Mean Filter, and Geometric Transformations.

Module 4: COMPRESSION - Image Compression Coding, Interpixel and Psycho visual Redundancy, Image Compression models, Elements of Information Theory, Error free comparison, Lossy compression, Image compression standards. Image Segmentation: Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation.

Module 5: REPRESENTATION AND DESCRIPTION - Representation, Boundary Descriptors, Regional Descriptors, Use of Principal Components for Description, Introduction to Morphology, Some basic Morphological Algorithms. Patterns and Pattern Classes, Decision-Theoretic Methods, Structural Methods

Text/ Reference Books:

1. Rafael C. Conzalez & Richard E. Woods, "Digital Image Processing", 2nd edition, Pearson Education, 2004.
2. A.K. Jain, "Fundamental of Digital Image Processing", PHI, 2003.
3. Rosefield Kak, "Digital Picture Processing", 1999.
4. W.K. Pratt, "Digital Image Processing", 2000.

M. Tech (VLSI Design) **Semester I**

MVL 115: MEMS & MICRO SYSTEM TECHNOLOGY

3L-0T-0P-3C **M.M.100**

Module 1: HISTORY OF MICRO-ELECTRO-MECHANICAL-SYSTEMS (MEMS) - Market for MEMS, MEMS Materials: Silicon and other materials , mechanical properties of materials- elasticity, stress and strain, Beams & Structures –cantilevers and bridges, point load & uniform loading, torsional, dynamic system; Piezoelectric & piezo resistive materials.

Module 2: MEMS FABRICATION PROCESSES - Review of IC fabrication process, Micromachining: Bulk micromachining (dry and wet etching), Surface micromachining (deposition, evaporation, sputtering, epitaxial growth), Deep RIE, Advanced Lithography, LIGA process; Multi User MEMS Process.

Module 3: MEMS DEVICES - MEMS Sensors and Actuators (Electrostatic, Electromagnetic, Thermal and Piezo), Bio-MEMS, Optical MEMS, Micro-fluidics MEMS;

Module 4: MEMS PACKAGING - MEMS packaging issues, die-level packaging, micro assembled caps & sealing.

Module 5: APPLICATION CASE STUDIES - MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micro mirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT), Air bag system, Micro motors, Scanning Probe Microscopy.

Text/ Reference Books:

1. Foundation of MEMS, Second Edition 2011 – Chang Liu, Pearson.
2. Gregory T A, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill,1998.
3. Microsystems Design – by Stephen D. Senturia, Publishers: Kluwer Academic / Springer, 2nd Edition (2005), ISBN: 0792372468
4. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 2002.

M. Tech (VLSI Design) **Semester I**

MDC 114: MICROWAVE INTEGRATED CIRCUITS

3L-0T-0P-3C **M.M.100**

Module I: METHODS OF ANALYSIS IN MIC

Introduction, Types of MICs and their technology, Propagating models, Analysis of MIC by conformal transformation, Numerical method, Hybrid mode analysis, Losses in microstrip, Introduction to slot line and coplanar waveguide.

Module II: COUPLERS AND LUMPED ELEMENTS

Introduction to coupled microstrip, Even and odd mode analysis, Branch line couplers, Design and Fabrication of lumped elements for MICs, Comparison with distributed circuits.

Module III: PASSIVE AND ACTIVE DEVICES

Ferrimagnetic substrates and inserts, Microstrip circulators, Phase shifters, Microwave transistors, Parametric diodes and amplifiers, PIN diodes, Transferred electron devices, Avalanche diodes, IMPATT, BARITT devices.

Module IV: MODULE-IV HIGH &LOW POWER CIRCUITS

Introduction, Impedance transformers, Filters, High power circuits, Low power circuits, MICs in Radar and satellite

Module V: MODULE-V FABRICATION METHODS

Fabrication process of MMIC, Hybrid MICs, Dielectric substances, Thick film and thin film technology and materials, Testing methods, Encapsulation and mounting of devices.

Text/ Reference Books:

1. Gupta K.C and Amarjit Singh, "Microwave Integrated Circuits", John Wiley, New York, 1975.
2. Hoffman R.K "Hand Book of Microwave Integrated Ciruits", Artech House, Boston, 1987
3. "Microwave Engineering" by Prof. GSN Raju, IK International Publishers, 2007
4. "Microwave Engineering" by P.A. Rizzi, PHI, 1999.
5. "Microwave Engineering: Non-reciprocal active and passive circuits" by Joseph Helszajin, McGraw Hill, 1992.

M. Tech (VLSI Design) **Semester I**

MDC 103: ADVANCE DIGITAL SIGNAL PROCESSING LAB USING MAT LAB

0L-0T-4P-2C **M.M.100**

List of Experiments:

1. Program to solve difference equations using conditional statements
2. Program for computing Linear and Circular Convolution using conditional statements
3. Program for up sampling and down sampling of a given sequence using conditional statements
4. Program for simulation of FFT using conditional statements and function calling
5. Program for designing Butterworth, Chebyshev type-I, Chebyshev type-II Analog and Digital Low pass, High pass, Band pass, Band stop filters using conditional statements and function calling
6. Program for designing Low pass, High pass, Band pass, Band stop filters using different Windowing techniques using conditional statements and function calling.
7. Program for Estimating Power Spectral Density of two sinusoids plus Noise Periodogram Estimation
8. Program for computing the convolution by overlap-add method
9. Program for computing the convolution by overlap save method
10. Program for Simulation of DPCM using Function Calling
11. Program for the solution of Normal Equations using Levinson –Durbin algorithm
12. Program for verification of sampling theorem using conditional statements.

M. Tech (VLSI Design) **Semester I**

MVL 102: SEMINAR-I (Review of Literature for Research)

0L-0T-4P-2C **M.M.100**

Students will be grouped in two to three, will have to decide final thesis area, download research papers from IEEE, ACM, Elsevier, Springer etc.

Summarizing Paper– Reading abstracts and finding ideas, conclusion, Advantages of Their approach, the drawbacks of the papers. Generalize results from a research paper to related research problems. Comparing the approach -Identify weaknesses and strengths in recent research articles in the subject. Practice sessions on how to read, analyze and summarize research papers. Students in group will have to deliver seminar, prepare a report and a review paper based on analysis.

M. Tech (VLSI Design) **Semester II**

MVL 201: CMOS VLSI DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: VLSI DESIGN FLOW, VLSI DESIGN STYLE AND FABRICATION PROCESS FLOW basic Steps, the CMOS n-well Process. Metal oxide semiconductor (MOS) structure, Types of MOSFET: Enhancement and Depletion. Structure and operation of MOS transistor. MOSFET process simulation.

Module 2: Basic operation of CMOS inverter, detailed analysis of its noise margin propagation delay, power dissipation concept of layout & area, layout optima zation & area estimation for a single as well as combinational logic circuits.

Module 3: DESIGN OF SEQUENTIAL LOGIC CIRCUITS - Static & dynamic latches registers, dynamic transmission gate, CMOS gate, pipelining approach for optimize sequential circuits; NDRA-CMOS pipelined structure, non-bistable sequential circuits, Schmitt trigger.

Module 4: Implementation strategies for digital ICs, introduction of custom and circuit design, hierarchy cell based design array based implementation, building blocks of adder, multiplier, shifter, barrel shifter, algorithmic shifter and other arithmetic operators, power speed tradeoff in data path structure.

Module 5: Design memory & array structure memory architectures & building blocks, address decoder, Sense amplifiers, driver/ buffers, timing control, power dissipation in memories, idea of testability and fault detection models.

Text/ Reference Books:

1. CMOS Digital Integrated Circuits Analysis, Sung-Mo (Steve) Kang, TMH
2. Essentials of VLSI Circuits and Systems, Kamran Eshraghian, Eshraghian, PHI
3. Introduction to VLSI Circuits and Systems, John P.Uyemura, John Wiley & Sons
4. Modern VLSI Design, Wayne Wolf, Pearson
5. Principles of CMOS VLSI Design, Neil H.E.Weste, Pearson
6. CMOS Logic Circuit Design, Uyemura, John P., Springer
7. VLSI Design, Shanthi, A. Kavitha, A., New Age International
8. VLSI Design and Technology, Bose, D.N., New Age International

M. Tech (VLSI Design) **Semester II**

MVL 202 ANALOG IC DESIGN

3L-1T-0P-3.5C **M.M.100**

Module 1: BASIC MOS DEVICE PHYSICS - MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, and MOSFET Noise.
Analog MOS Process: Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce.

Module 2: SINGLE STAGE AMPLIFIERS - Common Source Stage, Source Follower, Common Gate Stage, Cascade, Folded Cascade.
Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell.
Current Sources and Mirrors: Current Sources, Basic Current Mirrors, Cascade Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

Module 3: FREQUENCY RESPONSE OF AMPLIFIERS - Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.
Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

Module 4: FEEDBACK - General Considerations, Topologies, Effect of Loading.
Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.
Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.
Noise: Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

Module 5: SWITCHED-CAPACITOR CIRCUITS - Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.
Non Linearity and Mismatch: Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques, Reduction of Noise by Offset Cancellation.

Text/ Reference Books:

1. Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).
2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).
3. Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.
4. Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley (2008).

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M. Tech (VLSI Design) **Semester II**

MAT 155: ADVANCED MATHEMATICS

3L-1T-0P-3.5C **M.M.100**

Module 1: DIGITAL REPRESENTATIONS - Signals and Systems, Linear Time Invariant Systems, Arithmetic: Fixed and Floating point representation, IEEE 754 Floating point standards, Floating point arithmetic operations

Module 2: LAPLACE AND FOURIER TRANSFORMS - The Laplace Transform, Properties, The Fourier Transform, Properties of Fourier Transform, FourierTransform of Sequence (Fourier series) and its properties, Fourier analysis for Continuous and Discrete Time Signals.Digital

Module 3: MULTIDIMENSIONAL AND DISCRETE TRANSFORMS - Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms,1D and 2D- DFT, VLT, Z Transform and its properties.

Module 4: WAVELET TRANSFORM - Wavelet Transform: Continuous: introduction, C-T wavelets, properties, inverse CWT. Discrete wavelet transform and orthogonal wavelet decomposition using Harr Wavelets.

Module 5: OPTIMIZATION PROBLEM - Convex sets and functions.The SIMPLEX Algorithm-Forms of linear programming problem, geometry of linear programming, Organization of Tableau. Computational considerations for SIMPLEX Algorithm. Duality: Dual of linear programming, dual simplex problem, Primal-dual algorithm. Algorithms and Complexity-shortest path, max-flow, Dijkstra's algorithm, min-cost flow, algorithm for graph search and matching; spanning trees and matroids; Integer Linear programming, Greedy algorithm, approximation algorithms; branch-and-bound; dynamic programming.

Text/ Reference Books:

1. "Linear Algebra and its Applications", David C. Lay, 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005
2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier
3. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi
4. Digital Signal Processing: a practical approach, Emmanuel C Ifeachor, W Barrie Jervis, Pearson Education (Singapore) Pte. Ltd., Delhi
5. Wavelet transforms-Introduction to theory and applications, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education
6. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists, Murray R. Spiegel, MGH Book Co., New York
7. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK
8. Advanced Engineering Mathematics, JAIN, R K, IYENGAR, S R K, Narosa, NEW YORK
9. Signal processing with fractals: a Wavelet - based approach, Wornell, Gregory, PH, PTR, NEW JERSEY
10. Wavelet a primer, Christian Blatter, Universities press (India) limited, Hyderabad

M. Tech (VLSI Design) **Semester II**

MVL 211 VLSI TESTING AND DESIGN FOR TESTABILITY

3L-0T-0P-3C **M.M.100**

Module 1: PHYSICAL DEFECTS AND THEIR MODELING - stuck at faults; Bridging Faults; Fault collapsing. Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing.

Module 2: TEST GENERATION FOR COMBINATIONAL CIRCUITS - D-Algorithm, Boolean Difference, ODEM, and ATPG.

Module 3: RANDOM, EXHAUSTIVE AND WEIGHTED - Random Test Pattern Generations Aliasing and its Effect on Fault coverage.

Module 4 PLA TESTING - cross-point Fault Model, Test Generation

Memory testing: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques; Test Generation for Sequential Circuits. Scan Design. Scan path and LSSD, BILBO Concept of Redundancy, spatial redundancy, Time redundancy

Module 5: RECENT TRENDS IN VLSI TESTING - Genetic Algorithms, Parallel Algorithms, Neural Networks, nano scale testing

Text/ Reference Books:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub: Inspec/IEE, 1999
2. VLSI Test Principles and Architectures: Design for Testability by: Laung- Terng Wang; Cheng-Wen Wu; Xiaoqing Wen
3. Advanced Simulation and Test Methodologies for VLSI Design by Gordon Russell
4. VLSI Testing: Digital and Mixed Analogue/Digital Techniques by Stanley Leonard Hurst
5. N.H.E.Weste and K.Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition - Addition Wesley, 1993.
6. Jan .M.Rabaey, "Digital Integrated Circuits a design perspective", PHI 1st Edition, 1995.

M. Tech (VLSI Design) **Semester II**

MVL 212 NEURAL NETWORKS & FUZZY LOGIC

3L-0T-0P-3C **M.M.100**

Module 1: INTRODUCTION - Neural networks characteristics, History of development in neural networks principles, artificial neural net terminology, Model of a neuron, Topology.

Module 2: LEARNING METHODS & NEURAL NETWORK MODELS - types of learning, Supervised, Unsupervised, Re-enforcement learning. Knowledge, representation and acquisition. Basic Hop field model, Basic learning laws, Unsupervised learning, Competitive learning, K-means clustering algorithm, Kohonen's feature maps.

Module 3: ARTIFICIAL NEURAL NETWORKS - Radial basis function neural networks, Basic learning laws in RBF nets, Recurrent back propagation. Introduction to counter propagation networks, CMAC network, and ART networks.

Module 4: APPLICATIONS OF NEURAL NETS - Applications such as pattern recognition, Pattern mapping, Associative memories, speech and decision-making..

Module 5: FUZZY LOGIC - Basic concepts of fuzzy logic, Fuzzy vs. Crisp set, Linguistic variables,Membership functions, Fuzzy sets & Operations of fuzzy sets, Fuzzy IF- THEN rules,Variable inference techniques, De-Fuzzification, Basic fuzzy inference algorithm, Fuzzy system design, Antilock Breaking system (ABS), Industrial applications.

Text/ Reference Books:

1. B. Yegnanarayana, "Artificial Neural Networks"PHI
2. J.M. Zurada, "Introduction to artificial neural systems", Jaico Pub.
3. ROSS J.T, "Fuzzy logic with engineering application", TMH
4. Simon Haykin, "Neural Networks", PHI
5. Ahmad M.Ibrahim, "Introduction to applied Fuzzy Electronics",(PHI)
6. P.D. Wassermann, "Neural computing theory & practice", (ANZA PUB).

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M. Tech (VLSI Design) **Semester II**

MVL 213 COMPUTER AIDED VLSI DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: Introduction to VLSI Design methodologies and abstraction levels, Introduction to VLSI design automation tools, Introduction to algorithmic graph theory, Computational complexity, Tractable and Intractable problems, Combinational optimization, Hardware modeling, High level synthesis, Internal representation, allocation, assignment, scheduling.

Module 2: Scheduling algorithms, Integer linear programming, Hueristic: list scheduling & force-directed scheduling.
Layout Compaction – design rules – problem formulation – algorithms for constraint graph compaction – placement & partitioning algorithms.

Module 3: Floor planning concepts – shape functions and floorplan sizing – types of routing Problems. Simulation – gate level modeling and simulation – switch level modeling and simulation

Module 4 : INTRODUCTION TO VHDL - Digital system design process , Hardware simulation , Levels of abstraction , VHDL requirements , Elements of VHDL Top down design, VHDL operators ,Timing, Concurrency ,Objects and classes , Signal assignments ,Concurrent and sequential assignments.

Module 5: Modeling Techniques and Advance Topics Entity Declaration, Architecture Body, Process statement, Loop control statements, Multiple Processes, Delay Models, Signal Drivers, Block statements, Component declaration and Instantiation, Concurrent Assignment statements, Generics and Configuration, Subprogram, Overloading, Packages and Libraries, Design Libraries, Generate statements, Attributes, Hardware.

Text/ Reference Books:

1. Sabih. H. Gerez, "Algorithm for VLSI Design Automation Theory and Practice",
2. John Willey & Sons Ltd., 2004
3. Naveed Sherwani "Algorithms for VLSI Physical Design Automation", 3rd edition,
4. Springer International edition, 2005.
5. Giovanni De Micheli "Synthesis and Optimization of Digital Circuits", 1st Edition Mc
6. Graw Hill, 1994.
7. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson
8. Education Asia, 2009.
9. H Yosuff and S M Sait "VLSI Physical Design Automation Theory and Practice", Mc
10. Graw Hill Pub. , 1995.

MVL 214 SEMI CONDUCTOR MEMORIES

3L-0T-0P-3C **M.M.100**

Module 1: RANDOM ACCESS MEMORY TECHNOLOGIES - Static Random Access Memories (SRAMS): SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit Operation, Bipolar SRAM Technologies, Application Specific SRAMs.

Module 2: Silicon on Insulator (SOl) Technology, Dynamic Random Access Memories (DRAMs), DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Soft Error Failures in DRAMs, Application Specific DRAMs.

Module 3: NONVOLATILE MEMORIES - Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read-Only Memories (PROMs), Bipolar PROMs, CMOS PROMs, EPROMs , Floating-Gate EPROM Cell

Module 4: MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing, Nonvolatile Memory. Modeling and Testing, Application Specific Memory Testing

Module 5: SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS - General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory Reliability, Reliability, Modeling and Failure Rate Prediction, RAM Fault Modeling, Electrical Testing, Peusdo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, Application Specific Memory Testing.

Text/ Reference Books:

1. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability:
Wiley- IEEE Press, 2002.
2. Ashok K. Sharma, "Semiconductor Memories, Two-Volume Set", Wiley-IEEE Press, 2003.
3. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, & Reliability", Prentice Hall of India, 1997.
4. Brent Keeth, R. Jacob Baker, DRAM Circuit Design: A Tutorial, Wiley-IEEE Press, 2000.
5. Betty Prince, High Performance Memories: New Architecture DRAMs and SRAMs Evolution & Function, Wiley, 1999.

M. Tech (VLSI Design) **Semester II**

MVL 215 LOW POWER VLSI DESIGN

3L-0T-0P-3C **M.M.100**

Module 1: LOW POWER BASICS - Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Module 2: DEVICE & TECHNOLOGY IMPACT ON LOW POWER - Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. .

Module 3: LOW POWER DESIGN CIRCUIT LEVEL - Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Module 4: LOW POWER ARCHITECTURE & SYSTEMS - Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Module 5: LOW POWER CLOCK DISTRIBUTION - Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text/ Reference Books:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad,“Low-Power CMOS VLSI Circuit Design” Wiley,2000

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M. Tech (VLSI Design) **Semester II**

MVL 203 VLSI SIMULATION LAB

0L-0T-4P-2C **M.M.100**

CYCLE 1:

1. Digital Circuits Description using Verilog.
2. Verification of the functionality of designed Circuits using function simulator.
3. Timing Simulation for critical Path time calculation.
4. Synthesis of Digital Circuits.
5. Place and route techniques for major FPGA Vendors using Xilinx, Altera, Cypress etc.,
6. Implementation of Designed Digital Circuits Using FPGA and CPLD devices.

CYCLE 2:

1. MoS inverter DC Characteristics, AC Characteristics, Transient Analysis.
2. NMOS, PMOS Characteristics.
3. Layout basics- INV, NAND, NOR, EXOR, EXNOR.
4. Layout of adder, subtractor, multiplexer.
5. Layout Comparator.

For Experiments in cycle 2: 3,4,5: Draw the Schematics Perform Simulation, Extract the Layout, Run Physical Verification (DRC, LVS, PEX) and post layout simulation.

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M. Tech (VLSI Design) **Semester II**

MVL 204: SEMINAR-II (Review of Literature for Research)

0L-0T-4P-2C **M.M.100**

Each student will now continue to download further the research papers in the area, analyze, and allocate individually, the set of papers.

Literature survey Overview -What is literature survey, Functions of literature survey, maintaining a notebook, developing a Bibliography.

Methods of data collection –Observation, survey, contact methods, experimental,determining sample design Searching for publications –Publication databases, search engines and patent databases,Find some/all of the references for a given paper, including those that are not on the web.

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M. Tech (VLSI Design) **Semester II**

MGT 103 PROJECT FORMULATION & APPRAISAL

3L-0T-0P-3C **M.M.100**

Module 1 Introduction – project attributes; project life cycle; role of managers; Management – scheduling; Gantt charts; CPM; PERT; crashing; Generation of project ideas – resource allocation; environment analysis – PEST analysis, porter's model; analysis of strategic capabilities – value chain, BCG matrix, flexibility

Module 2 Appraisal methods in project scanning and selection – market appraisal; technical appraisal; environmental appraisal; evaluating intangibles, social appraisal – SCBA, UNIDO, LM, CSR.

Module 3 Total quality management: Introduction - Need for quality - Evolution of quality - Definition of quality -Basic concepts of TQM - Definition of TQM – TQM Framework -Contributions of Deming, TQM principles , The seven traditional tools of quality – New management tools – Six-sigma.

Module 4 **Financial Appraisal:** Time value of money; cost of capital – equity, debt, preference; weighted average cost; marginal and average cost; Capital budgeting – investment appraisal techniques; NPY; IRR; Payback period; replacement decisions; selection of exact discount factor – problems, inflation, taxation;

Module 5: **Risk Analysis** models – single probability analysis; sensitivity analysis; break even analysis; certainty equivalent; uncertainty analysis, simulation; decision tree model; risk and utility.

Recommended Books

1. Khatua Sitangshu. Project Management and Appraisal, Oxford University Press
2. Pandey, I.M. Financial Management. Vikas Publishing House
3. Prasanna, Chandra. Financial Management. Tata McGraw-Hill
4. Maheshwari, S .N. & Maheshwari, S. K. Advanced Management Accounting Vol.1 & Vol.2. Vikas Publishing House
5. Paresh Shah. Management Accounting. Oxford University Press

M. Tech (VLSI Design) **Semester III**

MVL 301: INTERNSHIP

0L-0T- (6Month) P+4C **MM 100**

As a part of the curriculum, the internship program forms an important component of education. It is an attempt to bridge the gap between an academic institution and the corporate world. The Program, which would be a simulation of real work environment, requires the students to undergo the rigor of professional environment for 180 days internship in relevant industry or recognized research organization. In the process, it provides an opportunity for the students to satisfy their inquisitiveness about the corporate world provides exposure to practicing professional skills as well as in research area and also helps them acquire social skills by being in constant interaction with the professionals of an organization. During internship, some of the students may be offered stipend and/or job offer by the company. This program benefits the student to understand what he/she has studied in the class room and what is being practiced in the industry.

Every student is required to undertake On-the-Job-Training (OJIT) in his/her domain area along with day-to-day functions of the company and may conduct his research work, both at the assistance and the execution level. This will help the student to gain a deeper understanding of the professional work, culture, organizational targets, delivering results, work pressure, etc. of an organization.

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M. Tech (VLSI Design) **Semester III**

MVL 302 DISSERTATION PART- I

0L+0T+0P+8C **MM 100**

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in Software ETAP/ MiPOWER / MATLAB / LABVIEW will be used. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute.Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.

Internal and external Continuous assessment:

	Guide	Evaluation Committee	
First Review	**30**	**20**	**Total**
Second Review	**30**	**20**	
Total	**60**	**40**	**100**

M. Tech (VLSI Design) **Semester III**

MVL 303: SEMINAR-III (REVIEW OF LITERATURE)

0L+0T+4P+2C **MM 100**

Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.

Individual students are required to choose a topic of their interest from Digital Communication Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Digital Communication Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

M. Tech (VLSI Design) **Semester IV**

MVL 401 DISSERTATION PART- II

0L+0T+P+16C **MM 100**

Objective: To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

Master Research project phase II is a continuation of project phase I started in the third semester. There would be two reviews in the fourth semester, first in the middle of the semester and the second at the end of the semester. First review is to evaluate the progress of the work, presentation and discussion. Second review would be a pre-submission presentation before the evaluation committee to assess the quality and quantum of the work done. This would be a pre qualifying exercise for the students for getting approval by the departmental committee for the submission of the thesis. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.